vJTAG Megafunction

# Architecture of JTAG

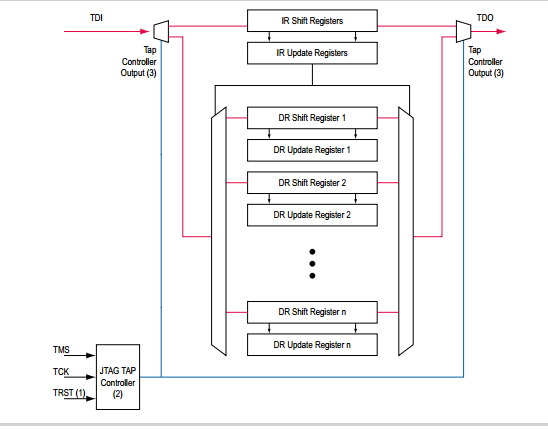
* DRs (Data Registers)
  + Primary data path
  + Carries the payload data for all transactions
  + Each chain has a dedicated function
    - Boundary scan cells form primary chain
    - Others are used for identification, bypassing the IC during boundary scan tests or custom use.
    - Megafunction allows you to extend the two DR chains to a user=defined custom application.
* IR (Instruction Register)
  + Used to select the bank of Data registers where the TDI and TDO must connect.
  + Functions as an address register for the bank of DRs.
  + Each instruction maps to a specific DR chain.
* State machine (Test Access Port (TAP) controller)
  + Used to arbitrate data
  + Major function is to route test data between the IR and DR register chains.
* 4 or 5 pin serial interface
  + TDI (Test data in)
    - Used to shift data into the IR and DR
  + TDO (Test data out)
    - Used to shift data out of the IR and DR
  + TMS (Test mode select)
    - Used as input to the TAP
  + TCK
    - Clock source of the JTAG
  + TRST
    - Reset the TAP (optional)
    - Also is not present on the Cyclone device family

Figure Functional Model of the JTAG Circuitry. From the ug\_virtualjtag.pdf

# SLD (System Level Debugging)

The SLD infrastructure defines the signaling convention and the arbitration logic for all programmable logic applications using a JTAG resource. The on chip debugging tools using JTAG resources share two DR chain paths (USER1 and USER0 instructions select the paths).

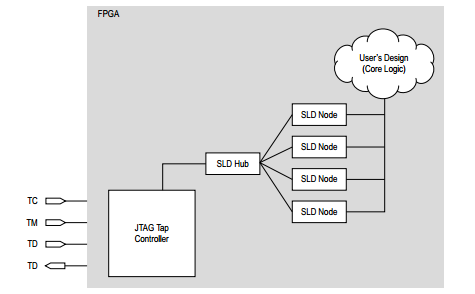


Figure System Level Debugging Infrastructure Functional Model

All components of the SLD infrastructure, except for the JTAG TAP are built using programmable logic resources. The SLD infrastructure consists of three subsystems:

1. JTAG TAP Controller
2. SLD hub
   1. Routes the TDI pin connection between each SLD node
   2. State machine that mirrors the JTAG TAP controller state machine
3. SLD nodes
   1. Represent the communication channels for the end applications.
   2. Each instance of IP requiring a JTAG communication resource, i.e. SignalTap II, would have its onwn communication channel (SLD node interface).
   3. Each node has its own IR and bank of DR chains.
   4. Up to 255 (8 bits) SLD nodes can be instantiated (depending on resources available).

The SLD hub and SLD nodes form a virtual JTAG scan chain within the JTAG protocol.

It is virtual in the sense that both the IR and DR transactions for each SLD node instance are encapsulated with a standard DR san shift of the JTAG protocol.

Since the SLD node IR and DR are a subset of USER1 and USER0 they are not part of the IR/DR registers set of the JTAG protocol. The SLD node registers are known as;

* VIR (Virtual IR)
* VDR (Virtual DR)

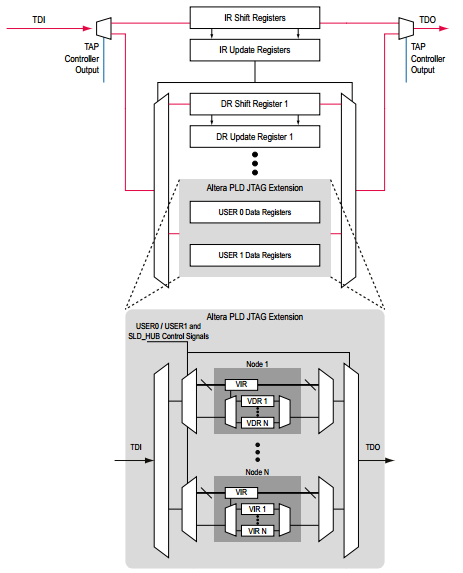


Figure Extension of the JTAG Protocol for the PLD Applications

## SLD Hub FSM

SLD hub decodes TMS independently from the JTAG TAP controller. The SLD Hub does the following;

* Enables an SLD node as the active path for the TDI pin
* Selects the TDI data between the VIR and VDR registers
* Controls that start and stop of any shift transactions
* Controls that data flow between the parallel hold registers and shift registers of both VIR and VDR.

The SLD hub uses the USER1 command to select the VIR data path and the USER0 command to select the VDR data path.

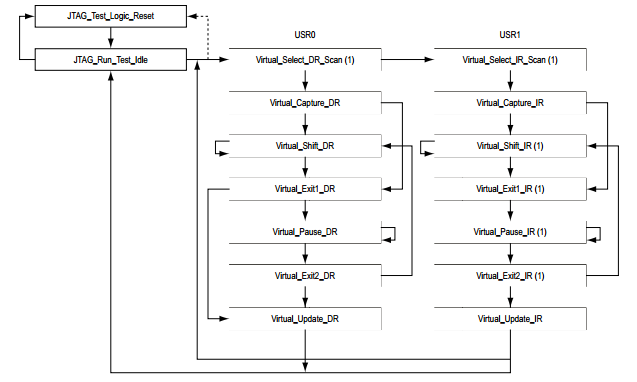
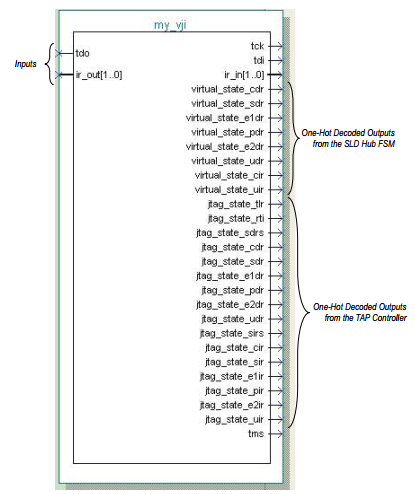


Figure sld\_hub Finite State Machine

# Virtual JTAG Interface

The vJTAG uses the SLD node interface, which provides communication to the JTAG port. The megafunction shows control signals that are part of the SLD hub;

* JTAG port signals
* All FSM controller states of the TAP
* SLD hub FSM

vJTAG provides a port interface that mirrors that actual JTAG ports. Ir\_in and ir\_out are parallel input and outputs to and from the VIR, where the VIR is used to select the active VDR datapath. All JTAG states and TMS are used for debugging purposes only.

The only functional elements from the virtual JTAG are the TDI, TDO, IR.

## Input Ports

|  |  |  |  |
| --- | --- | --- | --- |
| **Port name** | **Required** | **Description** | **Comments** |
| tdo | Y | Writes to the TDO pin on the device |  |
| Ir\_out[] | N | Virtual JTAG instructions register output. The value is captured whenever virtual\_state\_cir is high | Input port [SLD\_IR\_WIDTH-1..0] wide. Specify the width of this bus with the SLD\_IR\_WIDTH parameter. |

## Output Ports

Output ports for the Virtual JTAG Megafunction

|  |  |  |  |
| --- | --- | --- | --- |
| **Port name** | **Required** | **Description** | **Comments** |
| Tck | Y | JTAG test clock | Connected directly to the TCK device pin. Shared among all virtual JTAG instances |
| Tdi | Y | TDI input data on the device. Used when virtual\_state\_sdr is high. | Shared among all virtual JTAG instances |
| Ir\_in[] | N | Virtual Jtag instruction register data. The value is available and latched when virtual\_state\_uir is high. | Output port [SLD\_IR\_WIDTH-1..0] wide. Specify the width of this bus with the SLD\_IR\_WIDTH parameter. |

High-Level Virtual JTAG State Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Port name** | **Required** | **Description** | **Comments** |
| Virtual\_state\_cdr | N | Indicates the virtual JTAG is in Capture\_DR state. |  |
| Virtual\_state\_sdr | Y | Indicates that virtual JTAG is in SHIFT\_DR state. | In this state, this instance is required to establish the JTAG chain for this device. |
| Virtual\_state\_eldr | N | Indicates that virtual JTAG is in Exit1\_DR state. |  |
| Virtual\_state pdr | N | Indicates that virtual JTAG is in Pause\_DR state. | The Quartus II software does not cycle through this state using the Tcl command. |
| Virtual\_state\_e2dr | N | Indicates that virtual JTAG is in Exit2\_DR state. | The Quartus II software does not cycle through this state using the Tcl command. |
| Virtual\_state\_udr | N | Indicates that virtual JTAG is in Update\_DR state. |  |
| Virtual\_state\_cir | N | Indicates that virtual JTAG is in Capture\_IR state |  |
| Virtual\_state\_uir | N | Indicates that virtual JTAG is in Update\_IR state |  |

Low-Level Virtual JTAG State Signals

|  |  |  |  |
| --- | --- | --- | --- |
| **Port name** | **Required** | **Description** | **Comments** |
| Jtag\_state\_tir | N | Indicates that the device JTAG controller is in the Test\_Logic\_Reset state. | Shared among all virtual JTAG instances |
| Jtag\_state\_rti | N | Indicates that the device JTAG controller is in the Run\_Test/ Idle state. | Shared among all virtual JTAG instances |
| Jtag\_state\_sdrs | N | Indicates that the device JTAG controller is in the Select\_DR\_Scan | Shared among all virtual JTAG instances |
| Jtag\_state\_cdr | N | Indicates that the device JTAG controller is in the Capture\_DR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_sdr | N | Indicates that the device JTAG controller is in the Shift\_DR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_eldr | N | Indicates that the device JTAG controller is in the Exit1\_DR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_pdr | N | Indicates that the device JTAG controller is in the Pause\_DR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_e2dr | N | Indicates that the device JTAG controller is in the Exit2\_DR state. | Shared among all virtual JTAG instances |
| Jtag\_state\_udr | N | Indicates that the device JTAG controller is in the Update\_DR state | Shared among all virtual JTAG instances |
| Jtag\_state\_sirs | N | Indicates that the device JTAG controller is in the Select\_IR\_Scan state. | Shared among all virtual JTAG instances |
| Jtage\_state\_cir | N | Indicates that the device JTAG controller is in the Capture\_IR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_sir | N | Indicates that the device JTAG controller is in the Shift\_IR state. | Shared among all virtual JTAG instances |
| Jtag\_state\_elir | N | Indicates that the device JTAG controller is in the Exit1\_IR state. | Shared among all virtual JTAG instances |

|  |  |  |  |
| --- | --- | --- | --- |
| **Port name** | **Required** | **Description** | **Comments** |
| Jtag\_state\_pir | N | Indicates that the device JTAG controller is in the Pause\_IR state. | Shared among all virtual JTAG instances |
| Jtage\_state\_e2ir | N | Indicates that the device JTAG controller is in the Exit2\_IR state. | Shared among all virtual JTAG instances |
| Jtag\_state\_uir |  | Indicates that the device JTAG controller is in the Update\_IR state. | Shared among all virtual JTAG instances |
| Tms |  | TMS input pin on the device. | Shared among all virtual JTAG instances |

## Parameters

Parameters for the Virtual JTAG Megafunction

|  |  |  |  |
| --- | --- | --- | --- |
| **Parameter** | **Type** | **Required** | **Description** |
| SLD\_AUTO\_INSTANCE\_INDEX | String | Y | Specifies whether the Compiler automatically assigns an index to the Virtual JTAG instance. Values are YES or NO. Whe you specify NO, you can find the auto assigned value of INSTNACE\_ID in the quartus\_map file. When you specify NO, you must define INSTNACE\_INDEX. If the index specified is not unique in a design, the Compiler automatically reassigns an index to the instance. The default value is YES. |
| SLD\_INSTANCE\_INDEX | Integer | N | Specifies a unique identifier for every instance of alt\_virtual\_jtag when AUTO\_INSTANCE\_ID is specified to YES. Otherwise, this value is ignored. |
| SLD\_IR\_WIDTH | Integer | Y | Specifies the width of the instruction register ir\_in[] of this virtual JTAG between 1 and 24 if omitted the default is 1. |